AFRL-AFOSR-JP-TR-2017-0058

Innovative Ge Quantum Dot Functional Sensing and Metrology Devices

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08/21/2017
Final Report

Air Force Research Laboratory
AF Office Of Scientific Research (AFOSR)/ IOA
Arlington, Virginia 22203
Air Force Materiel Command

REPORT DOCUMENTATION PAGE

Form Approved
OMB No. 0704-0188

1. REPORT DATE *(DD-MM-YYYY)*	**2. REPORT TYPE**	**3. DATES COVERED** *(From - To)*
25-08-2017	Final	29 May 2015 to 28 May 2017

4. TITLE AND SUBTITLE
Innovative Ge Quantum Dot Functional Sensing and Metrology Devices

5a. CONTRACT NUMBER

5b. GRANT NUMBER
FA2386-15-1-4025

5c. PROGRAM ELEMENT NUMBER
61102F

6. AUTHOR(S)
Pei-Wen Li

5d. PROJECT NUMBER

5e. TASK NUMBER

5f. WORK UNIT NUMBER

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)
National Chiao Tung University
1001 TA HSUEH RD.
HSINCHU CITY, 30056 TW

8. PERFORMING ORGANIZATION REPORT NUMBER

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)
AOARD
UNIT 45002
APO AP 96338-5002

10. SPONSOR/MONITOR'S ACRONYM(S)
AFRL/AFOSR IOA

11. SPONSOR/MONITOR'S REPORT NUMBER(S)
AFRL-AFOSR-JP-TR-2017-0058

12. DISTRIBUTION/AVAILABILITY STATEMENT
A DISTRIBUTION UNLIMITED: PB Public Release

13. SUPPLEMENTARY NOTES

14. ABSTRACT
This project successfully developed cutting-edge fabrication technologies for (1) the growth and autonomous migration mechanism of Germanium (Ge) quantum dots (QDs) within SiO2, Si3N4, and even Si substrate, (2) the realization of innovative Ge QD/Si coupled-QD (CQD) photodetectors and Ge QD MOS phototransistors for visible to near IR photodetection, (3) the demonstration of direct bandgap photoluminescence from tensile-strained Ge QDs embedded within SiO2 system, and (4) self-organized Ge QD MOSFETs . Our designer Ge QDs embedded within Si-containing layers provide a great promise for Si-based light sources, photodetectors, and transducer amplifiers for Si-based photon/charge sensing, photonics, and even optical interconnections. Si-based photon/charge sensor, photonics, and optical interconnects have shown tremendous promises for replacing tight-packing, large latency electrical wires thanks to their inherent advantages of low energy, high data-rate transmission, and huge data capacity. It is therefore imperative to exploit the co-residency of optical interconnects systems and electronic circuits on a single-chip platform to provide high-performance functional-diversification CMOS Si integrated circuits. Motivation to employ Ge QDs for Si-based photonics is strong in light of its pseudo-direct gap electronic structure and the compatibility with Si CMOS technology.

15. SUBJECT TERMS
quantum, sensing, dot, QD, SET, optoelectronics, nano, devices, metrology

16. SECURITY CLASSIFICATION OF:			**17. LIMITATION OF ABSTRACT**	**18. NUMBER OF PAGES**	**19a. NAME OF RESPONSIBLE PERSON**
a. REPORT	**b. ABSTRACT**	**c. THIS PAGE**			WINDER, SHEENA
Unclassified	Unclassified	Unclassified	SAR	23	**19b. TELEPHONE NUMBER** *(Include area code)* +81-42-511-2008

Project Title: Innovative Ge Quantum Dot Functional Sensing/Metrology Devices

Period: May 26th 2015–May 25th 2017

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Abstract

Through this project, we have successfully developed cutting-edge fabrication technologies for (1) the growth and autonomous migration mechanism of Germanium (Ge) quantum dots (QDs) within SiO_2, Si_3N_4, and even Si substrate, (2) the realization of innovative Ge QD/Si coupled-QD (CQD) photodetectors and Ge QD MOS phototransistors for visible to near IR photodetection, (3) the demonstration of direct bandgap photoluminescence from tensile-strained Ge QDs embedded within SiO_2 system, and (4) self-organized Ge QD MOSFETs . Our designer Ge QDs embedded within Si-containing layers provide a great promise for Si-based light sources, photodetectors, and transducer amplifiers for Si-based photon/charge sensing, photonics, and even optical interconnections.

Si-based photon/charge sensor, photonics, and optical interconnects have shown tremendous promises for replacing tight-packing, large latency electrical wires thanks to their inherent advantages of low energy, high data-rate transmission, and huge data capacity. It is therefore imperative to exploit the co-residency of optical interconnects systems and electronic circuits on a single-chip platform to provide high-performance functional-diversification CMOS Si integrated circuits. Motivation to employ Ge QDs for Si-based photonics is strong in light of its pseudo-direct gap electronic structure and the compatibility with Si CMOS technology.

Introduction:

As the demands for on-chip functionality continuous to grow, it is widely recognized that metal-wired electrical interconnects is unlikely an effective solution to keep up with the performance roadmap of Moore's Law due to constraints of severe information latency and power consumption. In contrast, optical interconnects have shown tremendous promise for replacing electrical wires thanks to their

inherent advantages of low energy, high data-rate transmission, and huge data capacity. It is therefore imperative to exploit the co-residency of optical interconnects systems and electronic circuits on a single-chip platform to provide high-performance functional-diversification CMOS integrated circuits.

The key challenge for on-chip optical interconnects lies in the seamless integration of photonics and electronics in CMOS technology, which is extremely difficult due to the lack of high efficient Si light sources. Another primary challenge is the development of low power per bit receivers, of the order of 10fJ/bit or less, for on-chip communication. Achieving this requires low capacitance photodetectors as well as tight integration with optical waveguide and low capacitance receiver circuits. The electronic-photonic integration is a formidable task since the micrometer scale of photonics is significantly larger than the nanometer scale of electronic devices. In the conversion from photons to electrons by photodetectors, this size incompatibility often leads to substantial penalties in power dissipation, area, latency and noise.

Ge has become a promising candidate for active photonic devices on Si thanks to its pseudo-direct gap electronic structure and the compatibility with Si CMOS technology. Ge-on-Si photonics based on the direct-gap transition of Ge, such as waveguide-coupled photodetectors and electro-absorption modulators have also been demonstrated. If a Ge-on-Si diode laser can be implemented, all active photonic devices on Si can be fulfilled using Ge, which greatly simplifies monolithic electronic-photonic integration. The realization of high-performance Ge-based light sources as well as low-power, high-speed Ge photodetectors indeed requires the growth of direct-gap Ge, heterostructure engineering for efficient radiative recombination, resonant cavity design for optical gain enhancement, waveguided photodetection for minimal optical coupling loss, etc. All these tasks cannot be simply conducted in terms of bulk Ge technology, and it is no doubt that nanoscience and nanotechnology would offer substantial contributions for Ge-based lasers and photodetectors based on unique effects of quantum confinement and local resonance.

Experiment:

1. <u>Self-organized, gate-stacking heterostructure of SiO_2/Ge-dot/SiO_2/SiGe-channel formation.</u>

The gate-stacking structure is self-organized and formed in a single oxidation step of $Si_{0.85}Ge_{0.15}$ nano-pillars patterned over a buffer layer of Si_3N_4 on top of the n-Si substrate. During the high-temperature oxidation of the poly-SiGe nano-pillars, the Si content in the nano-pillar is preferentially oxidized, squeezing the remaining Ge radially inwards to the centers of the oxidized pillars. Further thermal oxidation results in the consolidation of the Ge nanocrystallites in each pillar via Ostwald Ripening into

single spherical Ge dots. These dots also simultaneously migrate through the underlying buffer Si_3N_4 layers and achieve contact with the Si substrate. Intriguingly, there is an approximately 3.5 nm-thick amorphous interfacial oxide layer surrounding the Ge dot. This interfacial oxide layer is conformal with the Ge dot and with the Si substrate below. Also, an approximately 20 nm-thick $Si_{1-x}Ge_x$ shell is generated within the Si substrate due to the migration of Ge interstitials to the Si substrate from the Ge nanodot, as shown in Figure 1. To reiterate, this entire, complex, heterostructure stack occurs within a single oxidation step.

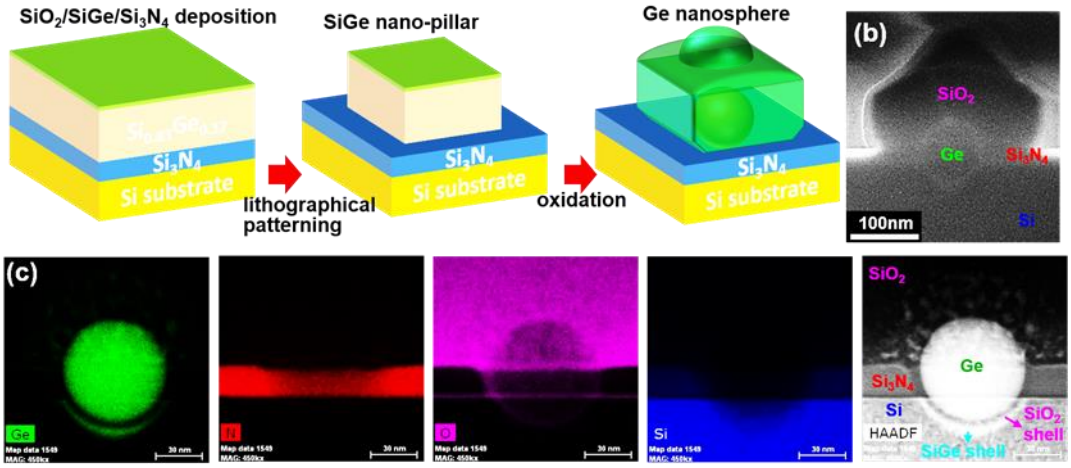

Figure 1 Heterostructure of Ge-nanosphere/SiO_2/SiGe-shell produced by thermally oxidizing SiGe nanopillar over buffer layers of Si_3N_4 on Si (100) substrate at 900°C for 25 min. followed by annealing at 875°C, 5minin an H_2O ambient. (a) schematics of experimental fabrication procedure, (b) cross-sectional scanning electron microscopy (C-SEM) and (c) EDX mapping micrographs.

2. <u>"Embedded Emitters": Microdisk-arrays of vertically-stacked Ge dots embedded within SiO_2</u>

We have advanced our growth technique to create arrays of vertically-stacked, tensile-strained Ge nanodots within SiO_2 with additional lithographic-patterning and post-anneal processing steps. Our fabrication process starts with a sequential, multi-layer deposition of 13nm-thick Si_3N_4, followed by 60nm-thick SiO_2, 500nm-thick undoped poly-$Si_{0.75}Ge_{0.25}$, and a topmost 50nm-thick Si_3N_4 over a Si substrate. This topmost Si_3N_4 is meant to provide a hard mask for subsequent lithographical patterning of the 150—260nm-wide SiGe "abacus"-nano-pillars containing multiple SiGe "beads" per pillar. The additional processing for producing abacus-profiles for the SiGe nano-pillars was achieved using successive cycles of SF_x plasma for etching away the SiGe alternately with CF_x plasma for sidewall passivation, as shown in Figure 2. Subsequently, thermal oxidation at 900 °C in an H_2O ambient converts the $Si_{0.75}Ge_{0.25}$ abacus-pillars to the desired geometry of vertically-stacked Ge-nanocrystallites layers within SiO_2. Following thermal oxidation, a conformal layer of Si_3N_4 is deposited to encapsulate the abacus-nano-pillars containing the alternating Ge nanocrystallites/SiO_2 layers. The nano-pillars are then subjected to 900°C

annealing in an O_2 ambient to facilitate Ostwald-Ripening (coarsening) of the originally small and irregularly-shaped Ge nanocrystallites into large, full-coalesced Ge nanodots. Finally, we lithographically fabricated microdisks, each containing an array of several nano-pillars with vertically-stacked, tens of nanometer-sized Ge nanodots embedded within SiO_2 matrices. The average diameter of these microdisks is 20μm.

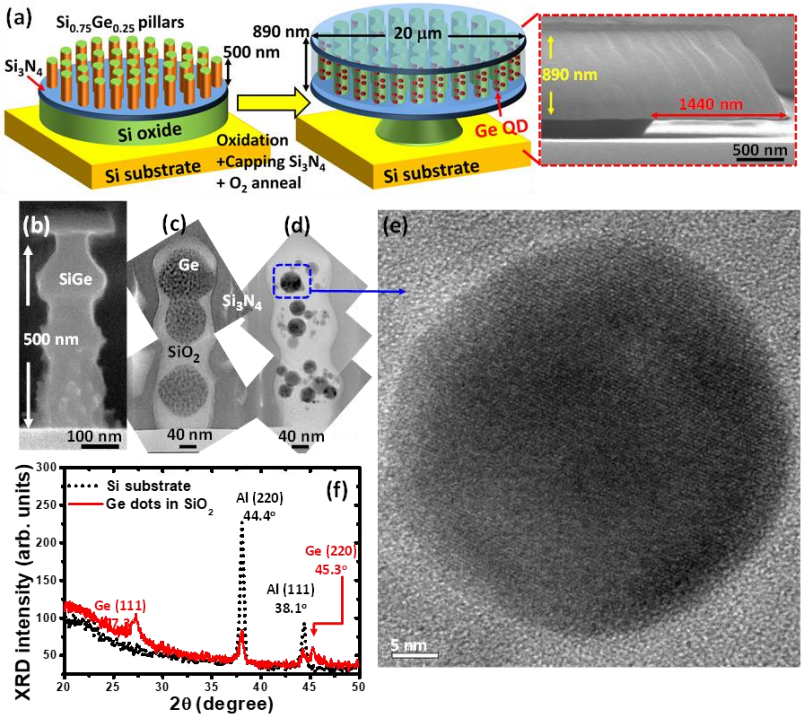

Figure 2 CSEM and CTEM micrographs of $Si_{0.75}Ge_{0.25}$ abacus-nanopillars, Ge-nanodot pillars, and microdisk pillar arrays. (a) Fabrication schematics and CSEM micrograph of the ultimate microdisk arrays of Ge nanodots. (b) $Si_{0.75}Ge_{0.25}$ abacus nanopillars lithographically formed by SF_6/C_4F_8 plasma etching, (c) as-formed clusters of small, irregularly-shaped Ge nanocrystallites within SiO_2 nanopillars following thermal oxidation of $Si_{0.75}Ge_{0.25}$ abacus-nanopillars, (d) Ostwald-ripening of Ge nanodots is facilitated by Si_3N_4 encapsulation and post annealing, (e) HRTEM of a single Ge nanodot, (f) XRD spectrum showing the high degree of crystallinity within the Ge nanodots. The presence of Al signals could be due to the background signals from the sample holder, since Al signals were also observed for the controlled sample of Si substrate.

3. Ge-dot PhotoMOSFETs fabrication.

The fabrication of Ge-dot PTs was initiated using n-Si(100) substrates with resistivity between 0.09–0.7 Ωcm. Following local oxidation isolation processes, BF_2 (1×10^{15} cm^{-2}, 40 keV) and phosphorus (1×10^{15} cm^{-2}, 30 keV) dopants were implanted for the formation of source/drain and substrate electrodes, respectively, for *p*-channel PTs. Next, a tri-layer deposition was conducted using sequential low-pressure chemical vapor deposition of 35nm-thick Si_3N_4, followed by 70 nm-thick poly-$Si_{0.85}Ge_{0.15}$, and finally a capping layer of 5 nm-thick SiO_2. The topmost SiO_2 layer is deposited for acting as a hard mask for the subsequent plasma etching to define SiGe nanopillars. The buffer Si_3N_4 layer between the $Si_{0.85}Ge_{0.15}$ nanopillars and the Si substrate serves as the initial, local source of Si interstitials for promoting the coalescence and migration

of Ge nanodots. This thin Si_3N_4 layer also acts as an oxidation mask to protect the Si substrate from being oxidized during the subsequent thermal oxidation of poly-$Si_{0.85}Ge_{0.15}$ nano-pillars. The topmost SiO_2/poly-$Si_{0.85}Ge_{0.15}$ layers were then lithographically patterned to create cylindrical poly-$Si_{0.85}Ge_{0.15}$ nano-pillars with a pillar density of 10^9–10^{10} cm^{-2} over the buffer Si_3N_4 layers. Next, thermal oxidation at 900 °C in an H_2O ambient for 28–50 min converts each poly-$Si_{0.85}Ge_{0.15}$ nano-pillar (100–210 nm in diameter) to a single spherical, 50–90 nm-diameter Ge dot that is positioned directly beneath each oxidized nano-pillar. A direct etch-back of the newly-formed SiO_2 layer over the Ge dots resulted in two thicknesses of 0nm and 35nm for the oxide above the Ge dots (Figure 3). It is interesting to note that there exists a 3.5 nm-thick interfacial layer of SiO_2 surrounding the Ge dots. This leads to two gate-oxide thicknesses (t_{ox}) of 3.5 nm and 38.5 nm for the Ge-dot gate stacks. Lastly, a 150 nm-thick indium tin oxide (ITO) layer was deposited and then patterned as a transparent gate electrode with gate-length (L_g) of 3 μm and gate-width (W) of 70 μm, followed by source/drain metallization and sintering processes to complete the device fabrication.

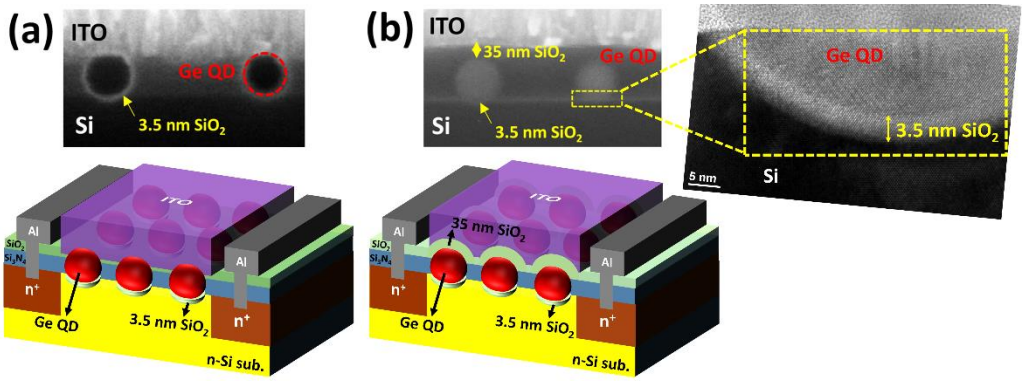

Figure 3 **Ge-dot phototransistors (PTs) have a self-organized, gate-stacking heterostructure of SiO_2/Ge-dot/SiO_2/SiGe-channel which is simultaneously produced in a single oxidation step.** Cross-sectional scanning electron microscopic micrographs and 3D schematic diagrams of Ge-dot PTs with (a) t_{ox} = 3.5 nm and (b) t_{ox} = 38.5 nm showing our ability to precisely control the sizes of the Ge nanodots, the thicknesses of the SiO_2 gate oxide. Notably, there exists a 3.5 nm-thick interfacial layer of SiO_2 surrounding the Ge dots as a result of an exquisitely-controlled dynamic balance between the fluxes of oxygen and silicon interstitials.

Results and Discussion:

1. <u>Self-organized, gate-stacking heterostructure of SiO_2/Ge-dot/SiO_2/SiGe-channel formation.</u>

We have reported successful demonstrations of CMOS-compatible, hybrid, lithographically-pattened/self-assembled approaches to not only deliberately grow size-tunable Ge nanospheres, but also to control their spatial locations within Si-based layers such as SiO_2, Si_3N_4, and even Si. These "designer" Ge nanospheres are generated using the exquisite control available through selective oxidation of poly-Si_{1-}

$_xGe_x$ nanopatterned-pillars grown over buffer layers of Si_3N_4 on Si substrates. During the high-temperature oxidation of the $Si_{1-x}Ge_x$ nano-pillars, the Si content of the $Si_{1-x}Ge_x$ nano-pillar is preferentially oxidized forming SiO_2. The remaining Ge is squeezed radially inwards to the core of the oxidized nano-pillar forming a cluster of irregularly-shaped Ge nanocrystallites. An intriguing discovery is that for a given Ge content within the $Si_{1-x}Ge_x$ nano-pillars that sit directly over buffer Si_3N_4 layers, further high-temperature thermal oxidation results in the "migration" and consolidation of the segregated, irregularly-shaped Ge nanocrystallites within each pillar into fully-coalesced, "spherical" Ge nanodots (Figure 1). These Ge nanospheres exhibit controllable migration through the underlying buffer Si_3N_4 layer. We believe this is because the Si_3N_4 layer acts as an initial, local source of Si interstitials that are released via a process of Ge-catalyzed, enhanced local oxidation of Si_3N_4. The emitted Si interstitials aid in both the migration and coarsening of these Ge nanocrystallites through Ostwald Ripening. The coalescing Ge nanocrystallites, in turn, further increase the generation of Si interstitials through the increased interfacial area for the catalytic decomposition of the Si_3N_4 layers. The surfaces of the growing Ge nanocrystallites act as "sinks" for these Si interstitials. Because of their affinity for Ge, the released Si interstitials migrate to the surface of the Ge nanocrystallites. Here, the Si facilitates the decomposition of surrounding oxide via the reaction: Si(interstitial) + $SiO_2(s) \rightarrow 2SiO(g)$. Oxide decomposition creates voids in front of the Ge nanocrystallite cluster promoting both Ostwald Ripening and the physical migration of the cluster or fully-coalesced Ge nanodot forward to the source of Si interstitials. Additionally, the oxygen interstitial concentration gradient (highest oxygen interstitial concentration at the oxide top surface) causes the Si interstitials and SiO to consequently migrate in the opposite direction to the Ge nanocrystallites, i.e. towards the source of higher oxygen interstitial concentration. The Si atoms and SiO are subsequently oxidized at the distal surface in the wake of the migrating Ge nanocrystallite, essentially backfilling SiO_2 behind the nanocrystallite, and thus further driving the downward migration of the nanocrystallite. It is a known fact that there is a 2.25x volume expansion when Si is converted to SiO_2. The regenerated SiO_2 layer expanding behind the Ge nanocrystallite and the voids created ahead of the nanocrystallite therefore propel the Ge nanocrystallite to migrate towards the source of the Si interstitials, namely the Si_3N_4 layers. Thus, these unique migration and Ostwald Ripening behaviors of the Ge nanodots are made possible by the "symbiotic" cooperation of Si, Ge and O interstitials resulting in a unique SiO_2 "Destruction-Construction" mechanism that promotes both the migration and the Ostwald Ripening.

2. <u>"Embedded Emitters": Microdisk-arrays of vertically-stacked Ge dots embedded within SiO_2</u>

HRTEM, *x*-ray diffraction (XRD), Raman, and PL spectroscopies were employed to examine the structural and optical properties of the Ge nanodots embedded within the SiO_2 layers. Figure 2(b—e) shows the results of cross-sectional scanning electron microscopy (CSEM) and cross-sectional transmission electron microscopy (CTEM) of the vertically-stacked Ge-nanodot array. It is seen that the consecutive etching/protection processes using SF_6 and C_4F_8 plasma respectively produces the resulting $Si_{0.75}Ge_{0.25}$ abacus-nano-pillars with three sets of beads (Ge nanocrystallite clusters) per pillar (Figure 2(b)). Thermal oxidation converts the SiGe abacus-pillars to have vertically-stacked clusters of 8—10nm Ge nanocrystallites embedded within oxide layers (Figure 2(c)). The subsequent encapsulation of the oxidized pillars by Si_3N_4 layers followed by post-annealing facilitates the consolidation of Ge nanocrystallites via an Ostwald-Ripening process in which the large nanocrystallites grow at the expense of small ones. Accompanying the completion of Ge nanocrystallite coalescence to form large Ge nanodots is the remarkable change in the morphology from irregular shapes to spherical shapes (Figure 2(d)). Most importantly, the crystallinity of the Ge nanodots is significantly improved during the Ostwald-Ripening process, as evidenced by the clear lattice fringes from HRTEM observations (Figure 2(e)) and by the diffraction peaks at 27.3° and 45.3° corresponding to Ge (111) and Ge (220), respectively, from XRD examination (Figure 2(f)).

Further experimental support for the high-quality crystallinity of the Ge nanodots embedded within the oxidized abacus-pillars is the appearance of strong longitudinal optical (LO) Ge-Ge phonon lines ranging from 299.75cm^{-1}–288.67cm^{-1} measured for Ge nanodots with corresponding sizes ranging from 67±5.8nm—32.4±7.8nm (Figure 4), which is in a sharp contrast to the observation of no measurable Raman line from the as-grown, 8–10nm Ge nanocrystallites. The absence of GeO_2 and Si/Ge intermixing signals with predicted spectral-shifts of 440cm^{-1} and 400—410cm^{-1}, respectively, is indicative of the chemical purity of the Ge nanodots embedded within the SiO_2 matrices. Also previous, extensive TEM-based *x*-ray Fluorescence measurements have confirmed that the nanodots are very nearly 100% Ge. In comparison to the Raman line of 301.5cm^{-1} measured for bulk Ge, significant red-shifts ($\Delta\omega$) of 1.75cm^{-1}, 5.8cm^{-1}, and 12.83cm^{-1} are observed for LO phonon lines arising from 67.0±5.8nm, 42.5±10.8nm, and 32.4±7.8nm-sized Ge dots, respectively. This suggests that the smaller Ge nanodots are subjected to increasing tensile-strain. We show that not only matrix-induced strain but also QCE do indeed modify the optical properties of our Ge nanodots embedded within SiO_2, as evidenced by their size-dependent PL wavelength measured for 32.4±7.8nm and for 42.5±10.8nm Ge nanodots respectively (Figure 3(a)). An analytical equation reported by Brus et al., predicting the QCE in nanodots, is given by $E = E_g + \frac{h^2}{8R^2}[\frac{1}{m_e^*} + \frac{1}{m_h^*}]$, where *E* is the

onset of absorption of the sample, E_g is the bulk band gap, ***R*** is the radius of the nanodot, ***h*** is the Planck constant, and m_e^* and m_h^* denote the effective masses of the electron and hole, respectively. For our 32.4±7.8nm and 42.5±10.8nm Ge nanodots, the estimated band-gap energies based on Brus's equation are 0.84±0.018 eV and 0.824±0.014eV, respectively, which are slightly less than our experimental PL peak-energies of 0.85eV and 0.835eV.

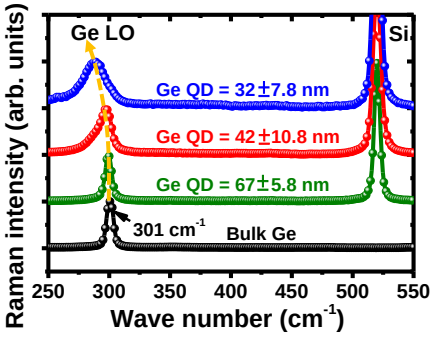

Figure 4 Raman spectra of 67.0±5.8 nm, 42.5±10.8 nm, and 32.4±7.8 nm Ge dots embedded within SiO_2 layers. A considerable redshift for the LO Ge-Ge phonon peak suggests that the smaller Ge nanodots are subjected to increasing tensile-strain. This observed result is consistent with our theoretical explanation that loss of mechanical coupling to the matrix accompanying Ostwald Ripening occurs when voids are created in the surrounding SiO_2 matrix in order for the nanodots to grow larger.

Further strong support for the combined effects of matrix-induced tensile-strains and QCEs in our Ge nanodots embedded within SiO_2 is the observation of strain-split direct bandgap transitions to the light-hole (LH) and heavy-hole (HH) valence bands (VBs) at energies of 0.82–0.85eV and 0.86–0.9eV, respectively, from our temperature- and power-dependent PL measurements made on our 32.4±7.8nm Ge nanodots. QCE and tensile-strain within our 32.4±7.8nm Ge nanodots greatly facilitate radiative recombination as evidenced by our experimentally observed PL peaks at approximately 1450–1500nm for measurement temperatures of 10–200K (Figure 5). In contrast, no significant PL emission was detected for as-formed Ge nanocrystallites, possibly because of enhanced non-radiative pathways due to their poor crystallinity offsetting the gains in direct bandgap transitions due to the higher tensile strains present in these as-formed nanocrystallites. High PL signal is obtained for the post-annealed Ge nanodots as a direct consequence of their improved crystallinity while still maintaining considerable tensile-strains due to their partial coherence with the surrounding SiO_2 matrices. An important observation derived from the temperature-dependent PL spectral results is the appearance of high-energy asymmetry when decreasing measurement temperature. The asymmetric PL spectra (drawn in dotted black color) measured for 32.4±7.8nm Ge nanodots at T = 10K appear to be well resolved into two separate Lorentzian curve-fits, i.e., a main peak centered at 0.85eV together with a satellite peak at 0.90eV, that are attributable to the direct bandgap

transitions from the Γ_{CB} to the LH ($\Gamma_{CB\text{-}LH}$) and to the HH ($\Gamma_{CB\text{-}HH}$), respectively. Both $\Gamma_{CB\text{-}LH}$ and $\Gamma_{CB\text{-}HH}$ transition PL peaks shift toward longer wavelength with increasing temperature (Figure 5(b)), following a Varshni-type equation of $E_D(T) = E_{D0} - \alpha T^2/(T + \beta)$. Figure 3(c) shows that the observation of measured $E_{D,\,\Gamma\text{-}HH}(T)$ values for our 32.4±7.8nm Ge nanodots being greater than direct bandgap PL energy of $E_{D,\,bulk\,Ge}(T)$ = 0.85-5.82×10$^{-4}T^2/(T+296)$ for bulk Ge is indicative of QC-enhanced energy bandgap, whereas $E_{D,\,bulk\,Ge}(T)$ landing well above the measured $E_{D,\,\Gamma\text{-}LH}$ curve is a consequence of the inherent tensile-strain within the Ge nanodots.

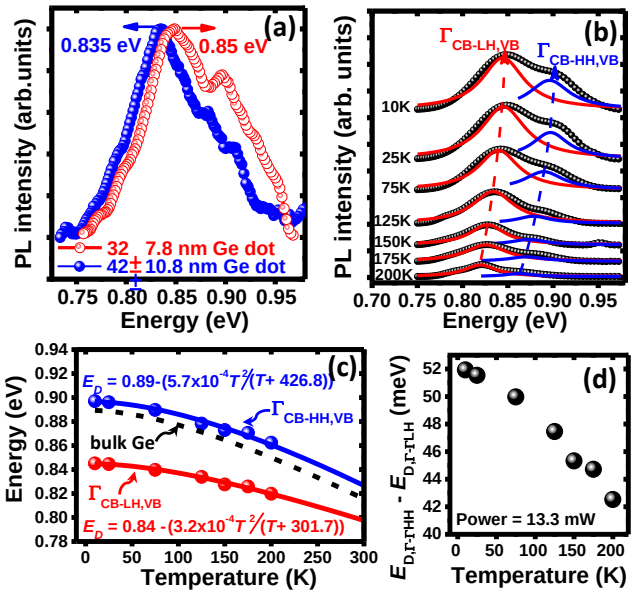

Figure 5 (a) PL spectra measured on 32.4±7.8nm and 42.5±10.8nm Ge nanodots at T = 10K. (b) Temperature-dependent PL spectra for 32.4±7.8nm Ge nanodots. Numerical curve fitting allows us to estimate the contributions of optical emission from the local minimum Γ valley in the conduction band (CB) to the absolute maximum light hole (LH) valence band (VB) as well as from the Γ point in the CB to the heavy hole (HH) VB. (c) Direct bandgap related PL peak energies (E_D) for 32.4±7.8nm Ge nanodots are plotted as a function of temperature from 10 to 200 K. The red and blue fitting curves are the calculated $E_{D,LH}$ and $E_{D,HH}$ related energies plotted as a function of temperature using Varshni's equation. Black, dash line denotes the calculated direct bandgap PL energy of $E_{D,\,bulk\,Ge}(T)$ = 0.85-5.82×10$^{-4}T^2/(T+296)$ for bulk Ge. (d) Measured separation energies, $E_{D,\,\Gamma\text{-}HH} - E_{D,\,\Gamma\text{-}LH}$, between the direct bandgap PL transitions from the Γ_{CB} valley to the HH and LH VBs for 32.4±7.8nm Ge nanodots.

We have also studied the excitation power dependence for the PL spectra of the 32.4±7.8nm Ge nanodots at 10K. Peak energies of both $\Gamma_{CB\text{-}LH}$ and $\Gamma_{CB\text{-}HH}$ at 0.85eV and 0.9 eV appear to be nearly unchanged with the excitation power (Figure 6(a)), which are consistent with previous work showing the power-independent PL behavior for the direct-bandgap transition for bulk Ge. The integrated PL intensity for the Ge nanodots increases monotonically with the excitation power, and a power law dependence of $I_{PL} \propto I_0^{\alpha}$ is extracted by numerically fitting the experimental data (Figure 6(b)). The fitted exponent values of α = 0.99 and 1.05 for $\Gamma_{CB\text{-}LH}$ and $\Gamma_{CB\text{-}HH}$ peaks, respectively, are very close to unity, indicating these two PL peaks are dominated by exciton radiative recombination within Ge nanodots instead of through Auger

recombination or trap processes, once again indicative of high-crystalline quality within the Ge nanodot. Another important finding is the predominance of PL from $\Gamma_{\text{CB-LH}}$ over $\Gamma_{\text{CB-HH}}$ transitions, and the relative intensity ratio $I_{\Gamma\text{-LH}}/I_{\Gamma\text{-HH}}$ linearly increases with decreasing excitation power. Possibly as the excitation power decreases, the relative population of photoexcited holes in the up-shifted LH becomes greater than that of the down-shifted HH band due to the reduced tail of the Fermi-Dirac distribution.

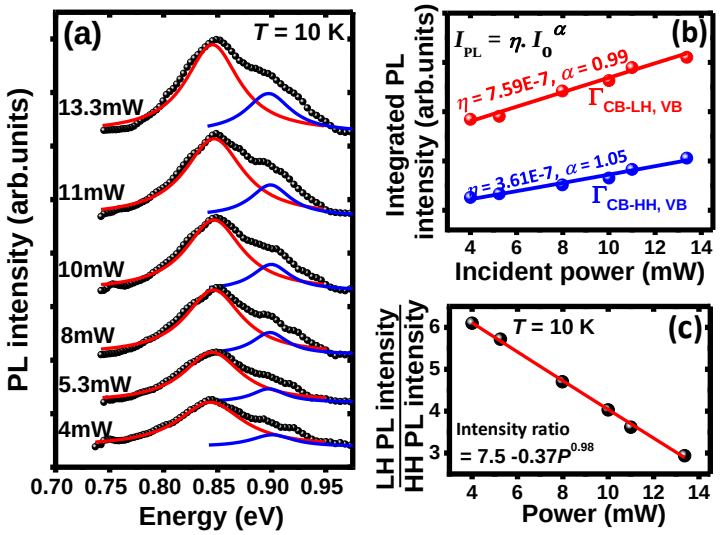

Figure 6 (a) Low-temperature PL spectra measured on the 32.4 7.8 nm Ge nanodots at different excitation laser powers ranging from 4 — 14 mW. Numerical fitting resolves two peaks centered at 0.845eV and 0.897eV, respectively. (b) The integrated PL intensity of both P1 and P2 peaks appears to have a linear dependence on the excitation laser power in a form of $I_{PL} \propto I_0$, and (c) Relative intensity of $I_{\Gamma\text{-LH}}/I_{\Gamma\text{-HH}}$ declines with increasing excitation power.

Determination of the excess carrier lifetime is crucial for the realization of efficient light-emitting devices. Figure 7 shows the temperature-evolution of transient direct-bandgap PL curves for the Ge nanodots from 10K to 100K. We analyzed the PL temporal behavior by fitting the experimental results using a double-exponential decay function, $I(t) = I_1\exp(-(t/\tau_1)) + I_2\exp(-(t/\tau_2))$, where $I(t)$ is the fluorescence intensity at time t, I_1 and I_2 are the fluorescence intensity at $t = 0$, and τ_1 and τ_2 are the characteristic lifetimes. For clarity, we denote the fast part of $I(t)$ by $I_1\exp(-(t/\tau_1))$ with a smaller decay time τ_1 in combination with a slower component of $I_2\exp(-(t/\tau_2))$ with a longer decay time τ_2. Excellent fits were achieved over approximately two decades of magnitude for all experimentally-measured, time-resolved data at various temperatures. For both $\Gamma_{\text{CB-LH}}$ and $\Gamma_{\text{CB-HH}}$ peaks, the ratios of $I_1\tau_1/I_2\tau_2$ are almost independent of measurement temperatures and are 10^4 and 10^2, respectively, indicating that our CW PL spectra are dominated by the fast component of $I_1\exp(-(t/\tau_1))$. The extracted decay times of $\tau_{1,\Gamma\text{-LH}}$ = 4.9–5.1ns and $\tau_{1,\Gamma\text{-HH}}$ =2.7–2.85ns remain nearly unchanged with temperature. Once again, the temperature-insensitive

decay time for both Γ-HH and Γ-LH transitions agrees with the observed PL at 0.9eV and 0.85eV originating from exciton radiative recombination. Thanks to the enhanced oscillator strength, the exciton lifetime of 2.7–5ns within our Ge nanodots is significantly shorter than the recombination lifetime of 30 μs measured for indirect-bandgap bulk Ge with no intentional dopants. Our Ge nanodots also exhibit comparable recombination lifetimes to that for $Ge_{1-x}Sn_x$ alloys (5ns) that are also dominated by interface recombination velocities.

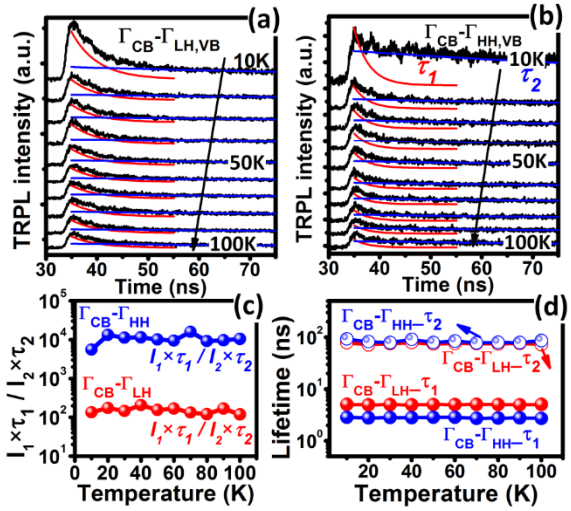

Figure 7 Time-resolved PL decays for PL peaks due to (a) Γ-LH and (b) Γ-HH recombination measured for 32.4±7.8 nm Ge nanodots over temperatures ranging from 10—100K, (c) Ratios of $I_1\tau_1/I_2\tau_2$ and (d) extracted carrier lifetimes for $\Gamma_{CB\text{-}LH}$, and $\Gamma_{CB\text{-}HH}$, respectively, are nearly constant over the 10—100K temperature range.

3. Ge-dot PhotoMOSFETs

Figure 8 shows I_D-V_G characteristics of 90nm-diameter Ge-dot p-MOSFETs biased at V_D = -2 V and measured either under darkness or variable-incident power (P_{IN}) 850 nm illumination. Ge-dot *p*-MOSFETs show typical transfer curves with ON-OFF current ratios (I_{ON}/I_{OFF}) of as high as 10^6 measured under darkness. One can clearly see that 850nm illumination does indeed increase drain current for the Ge-dot p-PTs across the entire experimental gate voltage range. For example, optical pumping at P_{IN} = 87.5μW significantly increases I_{ON} and I_{OFF} for Ge-dot *p*-PTs by a factor of 20 and 8×10^6 in magnitude, respectively, in comparison to the corresponding dark current values. This indicates that a high-level injection of photocarriers generates very high photocurrents that surpass thermionic and tunneling currents for both the ON- and OFF-states. In contrast, there appears to be a relatively small enhancement in I_{OFF} (at most 10x) and also no visible deviation in I_{ON} for the control Si-MOSFET (i.e., not containing Ge dots) under similar variable illumination conditions. Another important finding of note is that our Ge-dot PTs also exhibit distinct photocurrent enhancement for both ON- and OFF-states under variable-power 1310 nm and 1550 nm illumination.

For illumination with wavelength greater than 1100 nm, the photon energy is insufficient to excite electron-hole pairs within Si substrate. The experimental observation of photocurrent gain for our Ge-dot PTs for 1310nm and 1550nm illumination is conclusive proof that the Ge dots are optically active for NIR photodetection.

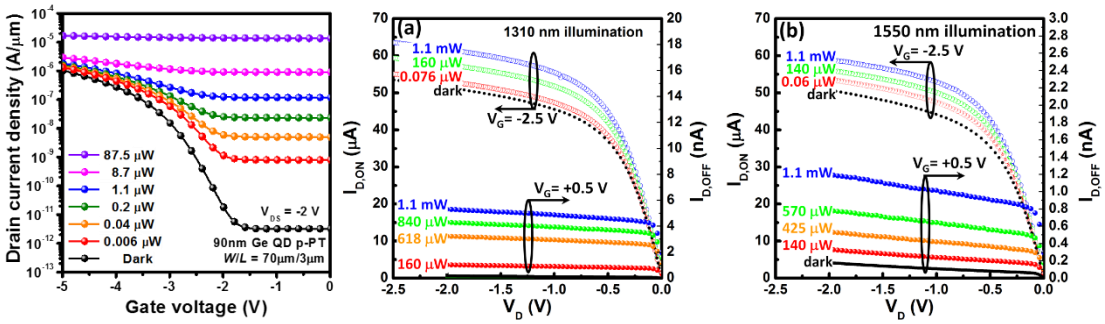

Figure 8 (a) I_D-V_G and (b) I_D-V_D characteristics of 90 nm Ge-dot *p*-PTs (W_g/L_g = 70 μm/3 μm) with $\boldsymbol{t}_{ox}$ = 38.5 nm under variable-power 850 nm and 1310/1550nm, respectively, illumination. Large photocurrent enhancement was achieved for our Ge-dot PTs when electrically-biased in the ON- and OFF-states based on the Ge dot mediating photovoltaic and photoconductive effects, respectively.

Under low-power 850 nm optical pumping, the $\Re$ of Ge-dot PTs appears to be well modulated by gate voltage as shown in Figure 9. For example, the photoresponsivity of 50 nm Ge-dot *p*-PT with $\boldsymbol{t}_{ox}$ = 38.5 nm measured at P_{IN} = 6 nW, increases from $\Re_{OFF}$ = 6 A/W at V_G = +1V (OFF-state) to $\Re_{ON} = 1.2\times10^3$ A/W at V_G = -2V (ON-state). The ON-OFF photoresponsivity ratio ($\Re_{ON}/\Re_{OFF}$) is further improved from 200 to 400 by reducing $\boldsymbol{t}_{ox}$ from 38.5nm to 3.5nm due to the improved gate modulation through a thinner gate-dielectric layer. The $\Re_{ON}$ of Ge-dot *p*-PT measured at P_{IN} = 6 nW also appears to improve with increasing Ge-dot diameter from 50 nm to 90 nm (Figure 9(a)). Figure 9(b) shows that for the 90 nm-diameter Ge-dot *p*-PT with $\boldsymbol{t}_{ox}$ = 3.5 nm, a very high $\Re_{ON}$ of 10^4 A/W is measured for 6 nW, 850 nm illumination with external quantum efficiency of EQE = $\Re[h\nu/e] = 1.5\times10^6$%. From the measured values of $\Re$, we are able to estimate a specific detectivity $D^* = \Re(A_{Gate}/2eI_{dark})^{0.5}$ at P_{IN} > 300nW, in which P_{IN} regime shot noise is predominant over other noise sources for Ge MOS structures. At P_{IN} = 300nW, the estimated values of detectivity for our Ge-dot PTs being electrically-biased at ON-state (V_G = -2.5V) and at OFF-state (V_G = +1V) are $D^*_{ON} \approx 1.2\times10^{11}$ cm/(W·s$^{1/2}$) and $D^*_{OFF} \approx 3.5\times10^{12}$ cm/(W·s$^{1/2}$), respectively. D^*_{OFF} appears to be significantly higher than D^*_{ON} primarily because of an extremely low dark current ($I_{dark,\ OFF} \approx 4.08\times10^{-11}$A versus $I_{dark,\ ON} \approx 5.95\times10^{-5}$A). $D^*_{OFF} \approx 3.5\times10^{12}$ cm/(W·s$^{1/2}$) for our Ge-dot PTs is comparable to the D^* value of 6×10^{12} cm/(W·s$^{1/2}$) for state-of-the-art Ge photodetectors measured at 600 nm.

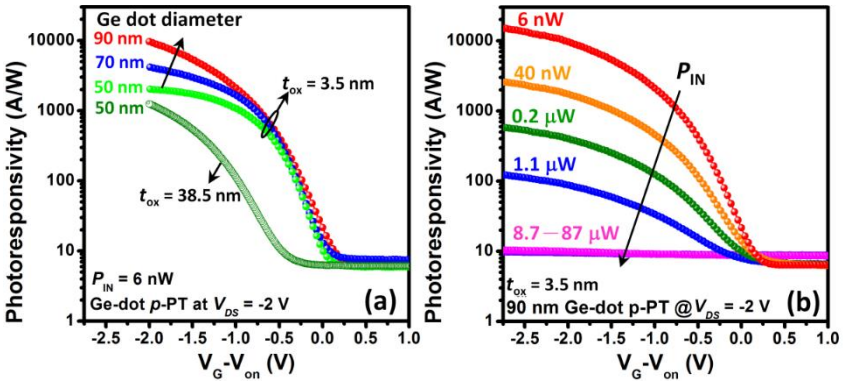

Figure 9 **Dependence of photoresponsivity ($\Re$) on gate voltage and light power.** (a) 50 – 90 nm-diameter Ge-dot *p*-PTs with t_{ox} = 3.5 nm and 38.5 nm under 6 nW, 850 nm illumination. The $\Re$ is well modulated by gate voltage and the ON-OFF photoresponsivity ratio is improved by increasing Ge-dot diameter from 50 nm to 90 nm and by decreasing t_{ox} from 38.5 nm to 3.5 nm. (b) 90 nm Ge-dot *p*-PT with t_{ox} = 3.5 nm under variable-power 850 nm illumination from 6 nW – 87 μW. $\Re_{OFF}$ shows a superior photocurrent linearity for P_{IN} ranging from 6 nW–1 mW, while $_{ON}$ decreases with increasing P_{IN} and approaches a saturation value of 10 A/W at $P_{IN} \geq$ 8.7 μW.

For 850 nm illumination, our 50–90 nm Ge-dot *p*-PTs biased at OFF-state exhibit a superior photocurrent linearity over a wide dynamic range for P_{IN} ranging from 6 nW–1 mW with a nearly constant value of $\Re_{OFF}$ = 6–10 A/W (Figure 9(b)). While very high $\Re_{ON}$ is measured for our Ge-dot PTs, $\Re_{ON}$ appears to have a strong dependence on the excitation power, i.e., the amplification for small optical signal is larger than that for large optical signals. Figures 9(b) and 10(a) show that for 50 – 90 nm-diameter Ge-dot *p*-PT with t_{ox} = 3.5 nm, $\Re_{ON}$ decreases with increasing P_{IN} and approaches a saturation value of 10 A/W at $P_{IN} \geq$ 10 μW for 850 nm illumination, thereby achieving a good photocurrent linearity for P_{IN} in the range of 9 μW–1 mW and possibly higher illumination power since 1mW is the maximum input power available to us given the limitations of our laser sources.

High $\Re_{ON}$ of 400 A/W and 300 A/W are also measured for 70 nm Ge-dot PTs at P_{IN} = 10 nW, for 1310 nm and 1550 nm illumination, respectively (Figure 10(b)). These $\Re_{ON}$ values are much higher than the reported values of 42A/W measured for Si/Ge heterojunction bipolar phototransistors (photoHBTs) at 1V bias. Our Ge-dot PTs exhibit power dependent photoresponsivity with the largest responsivity obtained for the sub-μW illumination regime for 850 nm–1550 nm wavelengths (Figures 10). The measured photoresponsivity decreases with increasing the optical power. This phenomenon is typically observed in phototransistors due to high light power affecting the gate and/or base potential.

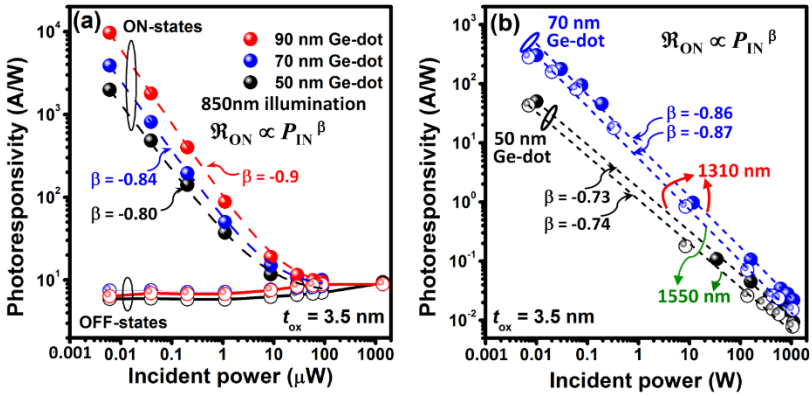

Figure 10 Power-dependent photoresponsivity of 50—90 nm Ge-dot *p*-PTs with t_{ox} = 3.5 nm under (a) 850 nm and (b) 1310 nm, 1550 nm illumination. Our Ge-dot PTs exhibit power dependent ON with the largest ON obtained for the sub- W illumination regime for 850 nm–1550 nm wavelengths. The decrease of $\Re_{ON}$ with increasing P_{IN} can be fitted by a power law of $\Re_{ON} \propto P_{IN}^{\beta}$ with β = -0.7—-0.9. The dashed lines are fitting curves and the circle symbols are experimental data.

Response time is an important figure of merit for photodetectors. The temporal response time of the Ge-dot PTs appears to be significantly improved by reducing the Ge-dot size from 90nm to 50nm as well as by decreasing t_{ox} from 38.5nm to 3.5nm (Figure 11). A response time of 0.48ns with a corresponding 3 dB frequency of 2.0GHz is measured for the Ge-dot *p*-PTs with Ge-dot size of 50nm and t_{ox} = 3.5nm. The response speed of the Ge-dot PTs is essentially determined by the lifetime of photo-generated carriers within the Ge dot and the gate RC delay that is primarily dominated by the thickness of gate oxide layer. For a given t_{ox}, the observation of faster response as measured for smaller Ge-dots, suggests better crystallinity with less defects for the smaller Ge dots.

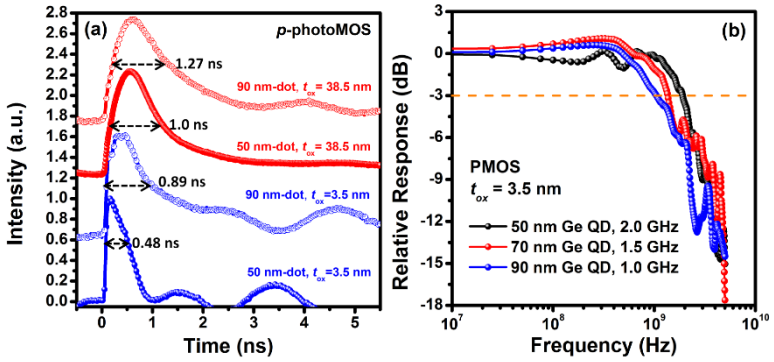

Figure 11 **Dynamical photoresponse of the Ge-dot *p*-PTs.** (a) Normalized temporal response time and (b) relative response to optical excitation as a function of frequency. Decreasing the Ge-dot diameter from 90 nm to 50 nm and reducing t_{ox} from 38.5 nm to 3.5 nm significantly improve the temporal response speed and the 3dB frequency bandwidth.

Project Outcome

We have successfully demonstrated high-photoresponsivity Ge-dot photoMOSFETs in a standard MOS configuration for the detection of 850–1550 nm

illumination. Each device has a self-organized, gate-stacking heterostructure of SiO_2/Ge-dot/SiO_2/SiGe-channel which is simultaneously fabricated in a single oxidation step. Superior control of the geometrical size and chemical composition for our Ge nanodots/SiO_2/$Si_{1-x}Ge_x$-shell MOS structure enables the practically-achievable, gate-stacking design for our Ge-dot photoMOSFETs. Both the gate oxide thickness and the diameter of the Ge dots are controllable. Large photocurrent enhancement was achieved for our Ge-dot photoMOSFETs when electrically-biased at ON- and OFF-states based on the Ge dot mediating photovoltaic and photoconductive effects, respectively. Both photoelectric conversion efficiency and response speed are significantly improved by reducing the gate-oxide thickness from 38.5 nm to 3.5 nm, and by decreasing Ge-dot size from 90 nm to 50 nm for a given areal density of Ge dots. Photoresponsivity values as high as 1.2×10^4 A/W and 300 A/W are measured for 10 nW illumination at 850 nm and 1550 nm, respectively. A response time of 0.48 ns and a 3 dB-frequency of 2 GHz were achieved for 50 nm-Ge-dot photoMOSFETs with channel lengths of 3 μm under pulsed 850 nm illumination.

Also we have demonstrated the fabrication of vertically-stacked Ge nanodots embedded within SiO_2 through the thermal oxidation of SiGe nanopillars followed by post-annealing under oxygen-deficient conditions. QCEs and tensile strains can be generated in the Ge nanodots embedded within SiO_2 matrices, facilitating direct bandgap PL from the Ge nanodots via strain-split direct-bandgap transitions to the LH and HH bands. Between $10-100$ K temperature-insensitive carrier lifetimes of 2.7ns and 5ns were measured for these transitions to HH and LH bands, respectively. Comprehensive theoretical calculations and modeling of strain, band structure and QCE are necessary as a follow up in order to quantitatively access the important contributions of QCE and strain effects on the PL from our Ge nanodots. We envisage further scientific exploration of our demonstrated tensile-strained Ge nanodots/SiO_2 system leading to the creation of advanced Ge high-performance light-emitting devices.

Published Journal Papers Published papers (Journal name, title, date):

1. M. H. Kuo, Meng-Chun Lee, Horng-Chih Lin, Tom George, and Pei-Wen Li, 2017, "High photoresponsivity Ge-dot photoMOSFETs for low-power monolithically-integrated Si optical interconnects," Scientific Report, 44402.
2. T. George, P. W. Li, K. H. Chen, K. P. Peng, and W. T. Lai, 2017 "Symbiotic" semiconductors: unusal and counter-intutive Ge/Si/O interactions," Journal of Physics D: Applied Physics, vol. 50, 105101. (2017/2)
3. M. H. Kuo, S. K. Chou, Y. W. Pan, S. D. Lin, T. George, and P. W. Li, 2016, "Direct bandgap photoluminescence from tensile-strained Ge nanodots embedded within

SiO_2," J. Appl. Phys., vol. 120, 233106 (2016)

4. Ching-Chi Wang, Wei-Ting Lai, Yi-Yeh Hsiao, Inn-Hao Chen, Tom George, Pei-Wen Li, 2016, "Geometry-dependent phase, stress state and electrical properties in nickel-silicide nanowires," Journal of Physics D: Applied Physics, vol. 49, 204102. (2016/4)
5. Chin-I Kuan, Horng-Chih Lin, Pei-Wen Li, and Tiao-Yuan Huang, 2016 "High-performance submicron ZnON thin-Film transistors with supreme field-effect mobility," IEEE Electron Device Lett., vol. 37, no. 3, 303.
6. Wei-Ting Lai, Kuo-Ching Yang, Po-Hsiang Liao, Tom George, and Pei-Wen Li, 2016, "Gate-stack engineering for self-aligned Ge-dot/SiO_2/SiGe-shell MOS capacitors," Frontiers in Materials, vol. 3, 00005.
7. Shuo-Huang Yuan, Zing-Way Pei, Pei-Wen Li, Yi-Jen Chan, 2015, "Au Nanoparticle Light Scattering Enhanced Responsivity in Pentacene Phototransistor for Deep-UV Light Detection," IEEE Electron Device Letters, vol. 36, 1186. (2015/11)
8. S.H. Yuan, Z. Pei, H.C. Lai, P.W. Li, and Y.J. Chan, 2015, "Pentacene phototransistor with gate voltage independent responsivity and sensitivity by small silver nanoparticles decoration," Organic Electronics, vol. 27, 7–11. (2015/8)
9. W. T. Lai, K. C. Yang, T. C. Hsu, P. H. Liao, T. George, and P. W. Li, 2015, "A Unique Approach to Generate Self-Aligned SiO_2/Ge/SiO_2/SiGe Gate-Stacking Heterostructures in a Single Fabrication Step," Nanoscale Research Letters, vol. 10, 224. (2015/05)
10. M. H. Kuo, W. T. Lai, S. W. Lee, and P. W. Li, 2015, "Design of multifold Ge/Si/Ge composite quantum-dot heterostructures for visible to near-infrared photodetection, Optics Letters, vol. 40, 2401-2404. (2015/5)
11. K. H. Chen, C. C. Wang, W. T. Lai, T. George, and P. W. Li, 2015, "The Pivotal Role of Oxygen Interstitials in the Dynamics of Growth and Movement of Germanium Nanocrystallites," CrystEngComm, vol. **17**, 6370 – 6375.

Paper currently under review (journal name, title, date accepted):

(1) Andriy Nadtochiy, Vasyl Kuryliuk, Oleg Korotchenkov, Pei-Wen Li & Sheng-Wei Lee, 2016, "Evidence for an enhanced thermoelectric performance of composite Ge/Si quantum dots,"submitted Scientific Reports.

(2) Chin-I Kuan, Horng-Chih Lin, Pei-Wen Li, and Tiao-Yuan Huang, 2016, "Performance Improvement of ZnO Thin-Film Transistors with ZnON Source/Drain Contacts,"

(3) Ming-Hao Kuo, Ping-Che Liu, Po-Yu Hong, Meng-Chun Lee, Horng-Chih Lin, Tom George, and Pei-Wen Li, 2017, "Very large photoresponsiviy and high photocurrent linearity for Ge-dot/SiO_2/SiGe photoMOSFETs under gate

modulation", submitted to APL Photonics.

12. Conference paper/poster/presentation (conf. name, title, date):

(1) M. H. Kuo, B. J. Liu, T. L. Huang, H. C. Lin, and P. W. Li, 2017, "Very large photogain and high photorespone linearity of Ge-dot photoMOSFETs operating in accumulation-mode for monolithic Si photonics," 2017 Silicon Nanoelectronics Workshop, Kyoto, June 4-6.

(2) C. Y. Hsueh, T. L. Huang, K. P. Peng, M. H. Kuo, H. C. Lin, and P. W. Li, "Counter-intuitive Ge/Si/O interactions and Ge/Si symbiosis enable the creatation of new classes of exciting nanoelectronic and nanophotonic devices" 2017 Silicon Nanoelectronics Workshop, Kyoto, June 4-6.

(3) Ming-Hao Kuo, M. C. Lee, J. W. Tien, Wei-Ting Lai, and Pei-Wen Li, "Optimal design of Ge-dot photoMOSFETs for highly-integrated monolithic Si Photonics", presented in Optical Fiber Conference, Los Angel, USA (March 19-23 2017)

(4) M. H. Kuo, Ming-Hao Kuo, Meng-Chun Lee, and Pei-Wen Li,, "High Photoresponsivity Germanium Nanodot PhotoMOSFETs for Monolithically-Integrated Si Optical Interconnects," 1st Electron Devices Technology and Manufacturing, Toyama, Japan (2017/2/28-3/2)

(5) C. W. Tien, P. H. Liao, K. P. Peng, H. C. Lin, and P. W. Li, "Channel engineering of self-organized Ge-nanosphere/SiO2/$Si_{1-x}Ge_x$-channel heterostructure on Si for Ge MOSFETs," oral presentation in 2016 International Electron Device and Material Symposium, Tainan, Taiwan.(2016/11/17-18)

(6) Po-Hsiang Liao, Shih-Cing Luo1, Kang-Ping Peng, Horng-Chih Lin, Tom George, and Pei-Wen Li, "Controllability of gate-stacking heterostructure of Ge gate/SiO_2/SiGe channel fabricated by one-step high temperature oxidation process", oral presentation in 2016 International Electron Device and Material Symposium, Tainan, Taiwan.(2016/11/17-18)

(7) Tom George, Pei-Wen Li, K. H. Chen, I. H. Chen, and W. T. Lai, "The Germanium Surprise! Unusual and Counter-Intuitive Ge/Si/O Interactions Result in Unique Nano-Optoelectronic Devices," oral presentation in 2016 International Electron Device and Material Symposium, Tainan, Taiwan.(2016/11/17-18).

(8) P. H. Liao, C. W. Tien, K. P. Peng, H. C. Lin, Tom George, and P. W. Li,, 2016, "Gate-stack engineering of self-organized nanospherical Ge gate/SiO_2/$Si_{1-x}Ge_x$ channel on Si (100) and Si (110) for Ge MOS devices," International Conference on Solid-State Devices and Materials, Sapporo, Japan (Sep. 25-30, 2016)

(9) M. H. Kuo, S. K. Chou, W. T. Lai,Y. W. Pan, S. D. Lin, Tom George, and P. W. Li, 2016, “Experimental observation of direct bandgap photoluminescence from tensile-strained Ge nanodots embedded within SiO_2 matrix,” International Conference on Solid-State Devices and Materials, Sapporo, Japan (Sep. 25-30, 2016)

(10) Ming-Hung Wu, Horng-Chih Lin, Pei-Wen Li, Tiao-Yuan Huang, 2016, “Film-Profile-Engineered IGZO Thin-Film Transistors with Gate/Drain Offset for High Voltage Operation,” 23rd IEEE International Symposium on the Physical and Failure Analysis of Integrated Circuits (IPFA 2016), Singapore, 18-21 July 2016

(11) Horng-Chih Lin, Chin-I Kuan, Pei-Wen Li, and Tiao-Yuan Huang, “Short-Channel ZnON Thin-Film Transistors with Film Profile Engineering,” 2016 Silicon Nanoelectronics Workshop, Honolulu, June 11-12.

(12) Horng-Chih Lin, Chen-Chen Yang, Yung-Chen Chen, Ruey Dar Chang, Pei-Wen Li, and Tiao-Yuan Huang, “Fabrication and RTN Characteristics of Gate-All-Around Poly-Si Junctionless Nanowire Transistors,” 2016 Silicon Nanoelectronics Workshop, Honolulu, June 11-12.

(13) M. H. Kuo, M. C. Lee, C. W. Tien, W. T. Lai, and P. W. Li, “Optimal design of Ge-dot photoMOSFETs for highly-integrated monolithic Si Photonics,” 2016 Silicon Nanoelectronics Workshop, Honolulu, June 11-12.

(14) P.W. Li (invited talk) 2016, “Designer Ge Quantum-Dot Phototransistors for highly-integrated, broadband optical interconnects,” IEEE INEC, Chengdu, China, May 9-11 2016.

(15) P. W. Li (invited talk) 2016, “Germanium quantum dots for functional sensing devices,” CSWNST 2016, Taipei, Taiwan (2016/03/23-24).

(16) R. J. Lu, T. Y. Huang, P. W. Li, and H. C. Lin, 2016 "High-gain, Low-voltage BEOL Logic Gate Inverter Built with Film Profile Engineered IGZO Transistors", oral presentation in VLSI-TSA, Hsinchu, Taiwan, 25-287 April, 2016.

(17) Horng-Chih Lin, Chin-I Kuan, Pei-Wen Li, and Tiao-Yuan Huang, “Short-Channel ZnON Thin-Film Transistors with Film Profile Engineering,” 2016 Silicon Nanoelectronics Workshop, Honolulu, June 11-12, 2016.

(18) Horng-Chih Lin, Chen-Chen Yang, Yung-Chen Chen, Ruey Dar Chang, Pei-Wen Li, and Tiao-Yuan Huang, “Fabrication and RTN Characteristics of Gate-All-Around Poly-Si Junctionless Nanowire Transistors,” 2016 Silicon Nanoelectronics Workshop, Honolulu, June 11-12, 2016.

(19) M. H. Kuo, M. C. Lee, C. W. Tien, W. T. Lai, and P. W. Li, “Optimal design of Ge-dot photoMOSFETs for highly-integrated monolithic Si Photonics,” 2016 Silicon Nanoelectronics Workshop, Honolulu, June 11-12.

(20) R. J. Lu, T. Y. Huang, P. W. Li, and H. C. Lin, 2016 "High-gain, Low-voltage

BEOL Logic Gate Inverter Built with Film Profile Engineered IGZO Transistors**",** oral presentation in VLSI-TSA, Hsinchu, Taiwan, 25-287 April, 2016.

(21) C. C. Wang, C. S. Jhou, C. L. Hsin, W. T. Lai, and P. W. Li, 2015, "Effects of array size- and Ge-content on cooling efficiency of poly-$Si_{1-x}Ge_x$ nanopillars thermoelectric coolers," oral presentation in 2015 International Electron Device and Material Symposium, Tainan, Taiwan.(2015/11/19–20)

(22) M. H. Kuo, S. K. Chou, W. T. Lai, Y. W. Pan, S. D. Lin, and P. W. Li, 2015, "Direct Bandgap Photoluminescence from SiO_2 Matrix Induced Tensile-strained Ge Quantum Dots," oral presentation in **2015 International Electron Device and Material Symposium, Tainan, Taiwan.** (2015/11/19–20)

(23) M. H. Kuo, S. Y. Hong, P. C. Chen, W. T. Lai, M. C. Lee, and P. W. Li, 2015, "Optimal Design and Fabrication of Germanium Dot Phototransistors for Optical Interconnects," oral presentation in **2015 International Electron Device and Material Symposium, Tainan, Taiwan.** (2015/11/19–20)

(24) Po-Hsiang Liao, Shih-Cing Luo, Kuo-Ching Yang, Tom George, W. T. Lai, and P. W. Li, "Gate-Stacking Engineering for Ge/SiO_2/$Si_{1-x}Ge_x$ MOS Devices," **2015 International Electron Device and Material Symposium, Tainan, Taiwan.** (2015/11/19–20)

(25) Ching-Chi Wang, Yi-Yeh Hsiao, Inn-Hao Chen, Wei-Ting La, Tom Georg, and Pei-Wen Li, "Geometry-dependent phase/stress and electrical resistivity in nickel-silicide nanowires," International Conference on Solid-State Devices and Materials, Sapporo, Japan (Sep. 27-30, 2015).

(26) Po-Hsiang Liao, Shih-Cing Luo, Kuo-Ching Yang, Tom George, W. T. Lai, and P. W. Li, "Gate-Stacking Engineering for Insta Ge/SiO_2/SiGe Metal-Oxide-Semiconductor Devices," International Conference on Solid-State Devices and Materials, Sapporo, Japan (Sep. 27-30, 2015).

(27) Wei-Ting Lai, Kuo-Ching Yang, Po-Hsiang Liao, Thomas George, and Pei-Wen Li, "Gate-stack engineering for self-aligned Ge-gate/SiO_2/SiGe-channel Insta-MOS devices", Silicon Nanoelectronics Workshop, Kyoto, Japan (June 14–15 2015)

(28) Ming-Hao Kuo, Ho-Chane Chen, Wei-Ting Lai, and Pei-Wen Li, "Characterization of carrier dynamics in Ge quantum dots through Ge quantum-dot MOSFETs using pulsed voltage technique," Silicon Nanoelectronics Workshop, Kyoto, Japan (June 14–15 2015)

4. Invited talks (event name, title, date):

(1) P. W. Li (invited talk) 2017, "Back to the Future: Germanium reemerges as the savior of Si opto-electronics," 13th CSWNST, Jiangyin, China (2016/04/20–22).

(2) P.W. Li (invited talk) 2016, “Designer Ge Quantum-Dot Phototransistors for highly-integrated, broadband optical interconnects,” IEEE INEC, Chengdu, China, May 9–11 2016.

(3) P. W. Li (invited talk) 2016, “Germanium quantum dots for functional sensing devices,” CSWNST 2016, Taipei, Taiwan (2016/03/23–24).

(4) Tom George, C. C. Wang, and P. W. Li, (Invited Talk) 2015, “Transition Metal Silicides: How to Expect the Unexpected!,” 2015 International Electron Device and Material Symposium, Tainan, Taiwan. (2015/11/19–20)

(5) Pei-Wen Li, (Invited Talk) 2015, “Innovative Ge quantum dot functional sensing/metrology devices,” Joint USAF-Korea NBIT-Taiwan Nanoscience Program Review, Seoul, Korea, Oct. 2015.

(6) Pei-Wen Li, (Invited Talk) 2015, “A novel CMOS approach to generate self-aligned SiO_2/Ge/SiO_2/SiGe gate-stacking heterostructures in a single fabrication step” in the 8th International Conference on Materials for Advanced Technologies (ICMAT), in Singapore, 28 June–03 July, 2015.

5. Award for best paper, best poster (title, date):

(1) M. H. Kuo, S. Y. Hung, P. C. Chen, W. T. Lai, M. C. Lee, and Pei-Wen Li, 2016 “Gate oxide thickness effect on germanium nanodot phototransistors for silicon-based optical interconnects”, oral presentation in 2016 International Electron Device and Material Symposium, Tainan, Taiwan.(2016/11/17–18) Best Poster Award.

(2) Po-Hsiang Liao, Shih-Cing Luo1, Kang-Ping Peng, Horng-Chih Lin, Tom George, and Pei-Wen Li, “Controllability of gate-stacking heterostructure of Ge gate/SiO2/SiGe channel fabricated by one-step high temperature oxidation process”, oral presentation in 2016 International Electron Device and Material Symposium, Tainan, Taiwan.(2016/11/17–18) Best Poster Award

6. IP disclosure/Patent/Patent submitted (title, date submitted):

(1) “Method for manufacturing gate stack structure in insta-metal-oxide-semiconductor Field-effect-transistor”, by Wei-Ting Lai, T. George, and P. W. Li, US patents, (Pending), Jan. 2015.

(2) “Method for manufacturing gate stack structure in insta-metal-oxide-semiconductor Field-effect-transistor”, by P. W. Li, Wei-Ting Lai, T. C. Hsu, K. C. Yang, P. H. Liao, and T. George, Taiwan patent, I531071, April 2016–July 2034.

(3) “Method for fabricating SiGe substrate,” by S. W. Lee, H. T. Chang, K. R. Lee, C. L. Hsin, and P. W. Li, Taiwan patent, I515772, Jan 2016–Sep 2033.

7. Visited AFRL/DoD installation in US, including under AOARD WoS program (Location, date):

(1) Dayton Ohio, April 6

(2) Seoul, Korea, Oct. 25 — Oct. 30.

(3) discussion with Sensors Directorate Dr. Rob Ewing on the collaboration subject: Double-QD micromaser